

Altera NIOS II SoPC

Standard Level - 3 days

Altera NIOS II SoPC is a 3-day course aimed at engineers who are using Altera technology to design Systems on Programmable Chip.

The course covers both hardware and software aspects of the design flow and is accessible to both hardware and software engineers. This co-training approach enables successful team working on SoPC designs, in that both software and hardware engineers gain an appreciation of the requirements of each other's discipline. This ensures successful convergence in the design flow and the development of efficient architectures.

The scope of the course includes an appreciation of the hardware platform, hardware-software partitioning, hardware acceleration as well as software development and debugging.

Altera NIOS II SoPC is developed and maintained for Doulos by specialist partner ALSE based on source material from Altera.

Doulos and ALSE are Approved Altera Training Partners.

Who should attend?

Design engineers who wish to learn how to use Altera technology for Systems on Chip.

What will you learn?

- Designing the hardware platform
- Software-hardware partitioning and co-operation
- Hardware acceleration techniques and integration
- Software development & debugging using Eclipse IDE
- Implementation of uCLinux

Pre-requisites

All participants must be computer literate and have a basic understanding of digital design. For the first day, a prior understanding of Quartus II is preferable, but not mandatory. For the third day, prior experience in C or C++ is preferable, but not mandatory.

Structure and Content

Day 1 - Building the Hardware Platform

Designing a System on a Programmable Chip (SoPC)

Why and when to use SoPC, available IPs, OpenCore, SoPC design flow • identifying standard and specific components • defining and customising the processor tightly coupled memories • the platform, data flows and signalling mechanisms

SoPC Builder

User interface • principles • step-by-step system generation • using the wizard and configuring the blocks

Hardware Platform Validation by HDL (Co)Simulation

Creating the simulation environment • interface with ModelSim • running the simulation

For further information contact your local Doulos [Sales Office](#).



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The Avalon Switch Fabric

The Avalon bus and interconnection system • miscellaneous kinds of peripheral ports and transfer modes • master with and w/o wait state • slave mode and wait states • generating the switch fabric • new features • adding custom peripherals • advantages and applications of custom instructions • several levels of customisation – combinational, multi-cycles, extended, internal, register file...

Multi-Masters and Direct Memory Access (DMA)

Avalon simultaneous multi-mastering Bus. Master/slave DMA transfers, streaming mode, Master arbitration scheme. Accelerating software execution.

Working with the Development Boards

Configuring the FPGA and loading the RAM and Flash memories • Typical SoPC board architecture • tips and techniques • restoring the factory default configuration

Day 2 - The Development Environment

The NIOS II Processor and Eclipse Design Flow

Main concepts • the Eclipse IDE • creating a software project • basic tools for compilation and debugging

Developing Programs for NIOS II

Introduction to the Hardware Abstraction Layer (HAL) and basic peripherals: alt_alarm timestamp and high-resolution timers

NIOS II Embedded Systems

System.h • updating the hardware configuration • memory mapping • stack, heap and boot sequence (alt_sys_init et alt_main) • hosted vs free-standing • optimising the code size • HAL and file system • managing the Flash memory • routines and interrupts

Advanced Debugging Techniques

Flash programming through Jtag • customising the user platform • The Jtag kernel • remote debugging (remote Jtag server) • optional debugging tools • debugging multi-processors systems • performance measurements and profiling tools • Using SignalTap II to aid with mixed hardware / software debugging

Day 3 - Advanced Concepts & Operating Systems

Custom Instructions and Hardware Acceleration – introducing C2H

Identifying the performance bottlenecks • creating and using custom instructions • hardware acceleration through dedicated custom hardware peripheral, without or with DMA transfers

Interfacing the Software and the Peripherals (Device Drivers)

HAL API interface • generic device models • creating and integrating the device drivers • initialisation and specific APIs • influence on data cache • The HAL formalism • extending drivers with your own

Software Components, Operating Systems and RTOS

Products currently available • MicroC/OS II • Lightweight IP stack and read-only zip file system •

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thread programming • impact on devices drivers

Embedded Linux: uCLinux

Locating the source and installation files • configuration • compilation • installation on Altera NIOS II board

Project services

Doulos Project Services enable clients to access our world-leading technical know-how and apply it directly to projects. **Expert-on-call**, **Expert-design** and **Expert-support** options can be flexibly packaged and delivered to provide valuable expertise and additional resource just when it is needed.

How to book a course

To make a provisional booking, or to obtain pricing information, please contact your local Doulos sales team. You will find contact details on our [website](#).

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