

# Altera Designing with Quartus II

## Standard Level – 3 days

**Altera Designing with Quartus II** is an intensive 3-day course aimed at engineers designing Altera® FPGAs, including the Cyclone® and Stratix® families. You will learn how to make best use of the latest features of the Quartus II software, including all the productivity and efficiency benefits of using TimeQuest Timing Analysis, Incremental Design and PowerPlay power analysis and optimisation.

Approximately 50% of class time is spent on practical exercises to reinforce the lectures. The exercises make use of a development board to emphasise the real-world application of the techniques that are learned.

Altera Designing with Quartus® II is developed and maintained for Doulos by specialist partner ALSE based on source material from Altera. Doulos and ALSE are **Approved Altera Training Partners**.

## Who should attend?

Existing users, who wish to become more productive by extending their knowledge of Quartus II and exploiting the latest features and techniques.

Design engineers who are new to Quartus II, and want quickly to get fully up to speed with all the key features of Quartus II. (Please see pre-requisites below).

## What will you learn?

- How to make best use of the full capability of the Quartus II software to implement your design.
- How to specify timing constraints and perform static timing analysis using TimeQuest.
- Use Incremental Compilation techniques, including creating LogicLock™ regions (Floorplanning) and Partitions to reduce compile times and more easily achieve timing closure.
- Estimating, analysing and optimising power consumption.
- Improve productivity and quality by automating the design flow using scripts.
- Functional and timing simulation using ModelSim®.
- Debugging designs using SignalTap® II and SignalProbe

## Pre-requisites

All participants must be computer literate and have a basic understanding of digital design.

The main course focus is on the more advanced features of Quartus II. A basic working knowledge of Quartus II would be beneficial, but is not absolutely essential. You can obtain this from the online tutorial included with Quartus II. This is also available online at [www.altera.com](http://www.altera.com).

## Course Content

### Quartus® II and the Design Flow

Review of Quartus II basics • Creating assignments & constraints • Dynamic checking • The Pin Planner • CSV import/export • Virtual pins • Creating and comparing revisions • Running Place and Route • Third party tool integration • Downloading and programming the target device • JTAG chains • Using non-Altera devices • Converting programming files and indirect JTAG programming (JIC)

# Altera Designing with Quartus II

## Standard Level – 3 days

### Advanced use of Quartus® II

Version-compatible databases • Optimisation options • WYSIWYG re-synthesis • Physical synthesis • Design analysis • Using the RTL, technology and state machine viewers • Cross-probing • Intelligent message suppression • Design rule checker (design rule assistant)

### Understanding and Mastering TimeQuest and SDC Constraints

The TimeQuest Static Timing Analyser • Concepts • Interface • Presentation of the Synopsys Design Constraints (SDC) format • SDC terminology • Using TimeQuest from the GUI and from SDC files • Understanding the TimeQuest reports • Practical applications to usual applications (constraining a single clock, input and output maximum and minimum delays, I/Os analysis, PLLs, etc..) • Early timing estimation

### Incremental Compilation

Preparing a project for incremental flow • Creating design partitions • Combining with floorplan constraints using LogicLock • Exporting and importing a design • Performance preservation • Top-down and bottom-up flows

### Power Analysis and Optimisation

Using PowerPlay • Early estimation & finer vector-based statistical estimation • Using the power optimisation adviser

### Design Flow Automation

For improved productivity and quality, design tasks and project management can be automated and secured with command-line scripts and Tcl scripts: Project creation • File management, archiving, cleanup, compilation, result testing, etc.

### Simulation

Functional simulation and post-layout timing simulation with ModelSim • Quick overview of ModelSim AE (Altera Edition) • RTL simulation, compilation & simulation scripts • Adapting the test bench to the timing model • Generation & compilation of the VITAL model & SDF file

### SignalTap® II and SignalProbe

Take advantage of free Embedded Logic Analysers to debug your design. The three modes • Configuration • Using the Logic Analysis Interface • Capturing/displaying • Saving data • Taking advantage of the segmented mode • Using the MegaWizard • Advanced Triggering • Signal Probe and the logic analyser interface • Purpose and use

### Design Space Explorer

Concepts & use

### In-System Memory Contents Editor

Concept and Use • Applications

Continued...

# Altera Designing with Quartus II

## Standard Level – 3 days

### Additional Options for In-house Delivery

Designing with Quartus II is available both as a publicly scheduled course and for in-house delivery. On scheduled courses, all the topics listed above will be taught. Additional exercises and optional topics may be taught at the course leader's discretion, depending on the time available and on the interests of the delegates.

For in-house delivery, there is more scope for customising the course contents. In particular, the following modules are available. Please call Doulos to discuss your requirements.

#### Techniques for Optimising Area and Timing

Making your RTL code more efficient • Optimising arithmetic • Resource sharing • Identifying and understanding the critical paths • Using the optimisation advisor • Physical synthesis and advanced options • Tips for improving RTL coding

#### Advanced Timing Analysis with TimeQuest

Advanced concepts • Recovery/removal analysis • Timing exceptions • Latency vs offset analysis • Fast corner analysis • Slack calculation • Timing driven compilation • Multiple clocks • Harmonics & derived clocks • Clock uncertainty • Multicycle path with hold • Early timing estimation

#### SignalTap® II

Advanced Triggering

#### Interfacing to External Memory

This module covers the use of Altera's memory interface IP, using the example of DDR memory: Customising and using a High Performance DDR memory controller in a Quartus II project • Verification using simulation, static timing analysis and in-system testing with SignalTap II • Understanding termination

### Project services

Doulos Project Services enable clients to access our world-leading technical know-how and apply it directly to projects. **Expert-on-call**, **Expert-design** and **Expert-support** options can be flexibly packaged and delivered to provide valuable expertise and additional resource just when it is needed.

### How to book a course

To make a provisional booking, or to obtain pricing information, please contact your local Doulos sales team. You will find contact details on our [website](#).

Altera, Stratix, Cyclone, SignalProbe and Quartus are trademarks of Altera Corporation.

For further information contact your local Doulos [Sales Office](#).

