

Essential Digital Design Techniques

Foundation Level - 2 days

Essential Digital Design Techniques is a fast-track, application orientated course designed to bridge the gap between text book theory and real world digital design practice.

It significantly accelerates the on-the-job learning curve for engineers new to digital design, or those needing to refine their design skills before project involvement. With a strong emphasis on practical design and hands-on workshops, this course has been specifically developed to capture design techniques usually learned over months, in an intensive 2-day format.

Essential Digital Design Techniques provides the ideal first stage in full scale project training for graduate design engineers, or engineers moving into digital design from other disciplines (including software or analog design). As such, it is the natural precursor to the Doulos **Comprehensive VHDL** and **Comprehensive Verilog** courses, which prepare engineers for HDL application within FPGA or ASIC design projects.

Who should attend?

- New graduate engineers embarking on a first project, or engineers with limited practical experience of digital design.
- Engineers from other disciplines (e.g. software design or analog design) re-training for digital design involvement, or requiring familiarisation with modern digital design techniques.

What you will learn?

- Combinational and Sequential Logic Design for PLDs and ASICs, with an emphasis on synchronous design techniques
- How to design and implement fundamental structures e.g. decoders, multiplexers, shift registers, counters
- How to design and implement synchronous Finite State Machines
- An overview of ASIC and field programmable logic design including a survey of state of the art devices
- Designing with programmable devices
- Effective Design methodologies and flows

PLEASE NOTE: this course does not teach, or require knowledge in a specific Hardware Description Language.

Pre-requisites

Delegates require no prior involvement in digital design projects or HDL knowledge, but should be familiar with the basic principles of digital electronics. Some background refresher reading can be suggested prior to the course if required (contact Doulos for details, or to discuss course suitability).

Course materials

Doulos course materials are renowned for being the most comprehensive and user friendly available.

Course Fees include:

- Fully indexed course notes creating a complete reference manual
- Workbook full of practical examples and solutions to help you apply your knowledge

For further information contact your local Doulos [Sales Office](#).



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Structure and content

Introduction

Designing with programmable logic and ASICs ♦ Synchronous design techniques ♦ First and second generation HDLs ♦ VHDL and Verilog ♦ Design process using HDLs

Digital Design Fundamentals

CMOS logic ♦ Representing bits and three-states ♦ Unsigned and signed (two's complement) numbers ♦ Static and dynamic definition of combinational logic ♦ Logic minimisation ♦ Avoiding asynchronous sequential logic

Synchronous Sequential Logic

Principles ♦ Using D-type flip-flops ♦ Characterisation – timing constraints ♦ Timing violations and metastability issues ♦ Timing performance of synchronous systems ♦ Static timing analysis ♦ Other flip-flop types

Introduction to Programmable Logic

Survey of programmable logic devices ♦ PLDs, CPLDs and FPGAs ♦ Programming ♦ Selecting an appropriate device ♦ Importance of the internal structure

Inputs and Outputs

I/O pin standards ♦ Pin assignment ♦ Dedicated pins ♦ Clocks and Resets ♦ Transmission line effects ♦ Electromagnetic Interference

Common Functions and their Implementation

Encoders and decoders ♦ Priority encoders ♦ Multiplexers ♦ Tristates used as Muxes ♦ Parity generator ♦ Shift Registers ♦ Johnson (ring) “counters” ♦ Linear Feedback Shift Registers

Arithmetic Structures

Half and full adders ♦ Large adders ♦ Carry lookahead adder ♦ Pipelining ♦ Synthesis of adders ♦ Counters ♦ Wide counters ♦ Binary to BCD conversion ♦ Serial arithmetic ♦ Importance of synchronous design

Synchronous Finite State Machines and Memories

Definition ♦ Graphical entry and symbolism ♦ Moore and Mealy structures ♦ Implementation ♦ State encoding and optimisation ♦ Using HDLs to design FSMs ♦ Using memories ♦ Memory types ♦ Using complex functions

Introduction to ASICs

ASIC types and technologies ♦ ASIC economics ♦ ASICs vs FPGAs ♦ Design for test ♦ Design process for ASICs

Follow-on courses

- Comprehensive VHDL
- Comprehensive Verilog

Book either course at the same time as Essential Digital Design Techniques and save 10% with the Doulos Fast-track Designer Induction.

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