

VHDL-AMS Workshop

Standard Level - 4 days

VHDL-AMS Workshop is a comprehensive 4-day class covering the extension to VHDL for analogue and mixed-signal modelling, as well as the underpinning VHDL knowledge required. It includes VHDL-AMS language features, with examples of electronic circuits and systems, and new constructs are explained with reference to circuit simulation algorithms.

The first 2-days of the class examine the VHDL language essentials; coding for register transfer level writing test benches, using VHDL tools and the VHDL design flow. Engineers already proficient in VHDL can omit the 'Introduction to VHDL' module and attend just the last 2-days.

The course is split between interactive classroom-style lectures and practical hands-on exercises using a commercial simulation tool. The workshops are carefully designed to reinforce the material presented, and illustrate the scope of the language, with interesting exercises.

Who should attend?

- Engineers who wish to extend their knowledge of VHDL to the modelling of analogue and mixed-signal electronic circuits.

What will you learn?

- The essential syntax and semantics of the VHDL language
- How to write VHDL test benches in order to verify the functionality of your design
- How to write high quality VHDL code that reflects best practice in the industry
- How to organise design files and design flow in a VHDL based project
- How to use VHDL with the simulation tool of your choice
- The essential syntax of the VHDL-AMS language
- The semantics of VHDL-AMS with respect to circuit and mixed-signal simulation
- How to model basic electronic components
- How to model larger mixed-signal systems
- How to model at both circuit level and signal-flow level
- How to combine VHDL-AMS models with legacy models

Pre-requisites

Knowledge of SPICE or other analogue simulation tools would be advantageous, but is not essential. Some basic circuit theory will be used and a familiarity with the general concepts *such as Kirchhoff's laws) would be helpful.

Training materials

Doulos training materials are renowned as the most comprehensive and user friendly available. Their style, content and coverage is unique in the HDL training world, and has made them sought after resources in their own right. Course fees include:

- Fully indexed course notes creating a complete reference manual
- VHDL Golden Reference Guide; pocket companion full of syntax, hints, tips and 'gotchas' (4-day class attendees only)

For further information contact your local Doulos [Sales Office](#).



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- Workbook full of practical examples to help you apply your knowledge. This includes a tool tour guide (to support the VHDL-AMS simulation tool used in the practical sessions).

Structure and content

Introduction to VHDL (days 1-2)

Introduction

The scope and application of VHDL ♦ Design flow ♦ Benefits ♦ Tool and Technology independence ♦ The VHDL world

Design Entities

The basic VHDL language constructs

Files and Libraries

The proper organisation and use of VHDL source files and libraries ♦ The compilation procedure

Processes

The process statement and its consequences for simulation and modelling

Sequential Statements

If, case and loop statements ♦ combinational logic and transparent latches ♦ generating test vectors

Types

Defining new data types ♦ modelling tri-state busses ♦ manipulating vectors, using operators ♦ conversion functions ♦ standard packages

More on Types

Making best use of integers and arrays ♦ modelling memories

More on Design Entities

Parameterising designs for re-use ♦ concurrent coding styles ♦ using assertions to report errors

Subprograms

Procedures and functions in test benches and RTL code ♦ understanding packages ♦ operator overloading

VHDL-AMS Workshop (days 2-4)

Introduction

Review of VHDL 1076-1999 Maths package 1076.2 ♦ Signal flow modelling in VHDL 1076.1 (VHDL-AMS) background

Nature, Terminal, Quantity

Definition of a nature ♦ Terminal nodes ♦ Free quantities ♦ Across and through quantities ♦ Electrical package

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Simultaneous Statements

Simultaneous statements ♦ Implicit quantities ♦ Solvability ♦ simultaneous if and case statements ♦
Examples: resistor, capacitor, diode

Netlists

Terminal and quantity ports ♦ Component instantiation ♦ Signal flow modelling

Procedural Statements

Sequential programming constructs ♦ Equivalent simultaneous statements ♦ Equivalent functions
Examples: MOSFET, Opamp

Mixed-Signal Simulation Cycle

Simulation cycle ♦ Initialisation ♦ Break statements ♦ Time step control ♦ Frequency and Noise domain modelling

Mixed-Signal Modelling

Mixing concurrent and simultaneous constructs ♦ Events ♦ Examples: ADC, DAC

Pros and Cons of VHDL-AMS

Limitations ♦ Future of VHDL ♦ Object-oriented VHDL ♦ Future of VHDL-AMS

Related courses

- VHDL for FPGA Design

Project services

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How to book a course

To make a provisional booking, or to obtain pricing information, please contact your local Doulos sales team. You will find contact details on our [website](#).