

VHDL for FPGA Design (Altera)

Foundation Level - 3 days

VHDL for FPGA Design (Altera) is a 3-day hands-on class, preparing engineers for practical project readiness for Altera FPGA designs. It provides basic training in the VHDL language, coding for RTL synthesis, exploiting architectural features the target device, writing test benches and using VHDL tools and the VHDL design flow. Delegates take away a flexible project infra-structure which includes a set of scripts, example designs, modules and constraint files to use, adapt and extend on their own projects.

While the emphasis is on the practical VHDL-to-hardware flow for Altera FPGA devices, this module also provides an excellent foundation for studying the more advanced features and application of VHDL required by both ASIC and FPGA designers.

Because Doulos is an independent company, delegates can use their choice of design tools during the workshops; the full range of VHDL simulation, synthesis and programmable logic design tools are supported. The workshops are based around carefully designed exercises to reinforce and challenge the extent of learning, and comprise approximately 50% of class time.

Who should attend?

- Engineers who wish to become skilled in the practical use of VHDL for Altera FPGAs
- Engineers who are about to embark on the first VHDL design project
- Engineers who have already acquired some practical experience in the use of VHDL, but wish to consolidate and extend their knowledge within a training environment

What will you learn?

- The VHDL language concepts and constructs essential for Altera FPGA design
- How to write VHDL for effective RTL synthesis
- How to target VHDL code to a Altera FPGA device architecture
- How to write simple VHDL test benches
- The tool flow from VHDL through simulation, synthesis and place-and-route
- How to write high quality VHDL code that reflects best practice in the industry

Pre-requisites

Delegates must have attended **Essential Digital Design Techniques** or an equivalent course, or have a good working knowledge of digital hardware design. No previous knowledge of VHDL or a software language is required.

Course materials

Doulos course materials are renowned for being the most comprehensive and user friendly available. Their style, content and coverage is unique in the HDL training world and had made them sought after resources in their own right. Course fees include:

Continued...

For further information contact your local Doulos [Sales Office](#).



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- Fully indexed course notes creating a complete reference manual
- Workbook full of practical examples and solutions to help you apply your knowledge
- Doulos Golden Reference Guide for VHDL language, syntax, semantics and tips
- Design flow guide for the Altera tool flow, including simulation, synthesis, place-and-route
- PaceMaker Tutorial & Reference – multi-media CD-ROM for optional pre-course preparation

Structure and Content

Introduction

The scope and application of VHDL • Design and tool flow • FPGAs • The VHDL world

Getting Started

The basic VHDL language constructs • VHDL source files and libraries • The compilation procedure • Synchronous design and timing constraints

FPGA Design Flow (Practical exercises using a hardware board)

Simulation • Synthesis • Place-and-Route • Device programming

Design Entities

Entities and Architectures • Std_logic • Signals and Ports • Concurrent assignments • Instantiation and Port Maps • The Context Clause

Processes

The Process statement • Sensitivity list versus Wait • Signal assignments and delta delays • Register transfers • Default assignment • Simple Testbenches

Synthesising Combinational Logic

If statements • Conditional signal assignments and Equivalent process • Transparent latches • Case statements • Synthesis of combinational logic

Types

VHDL types • Standard packages • Integer subtypes • Std_logic and std_logic_vector • Slices and concatenation • Integer and vector values

Synthesis of Arithmetic

Arithmetic operator overloading • Arithmetic packages • Mixing integers and vectors • Resizing vectors • Resource sharing

Synthesising Sequential Logic

RISING_EDGE • Asynchronous set or reset • Synchronous inputs and clock enables • Synthesisable process templates • Implied registers

FSM Synthesis

Enumeration types • VHDL coding styles for FSMs • State encoding • Unreachable states and input hazards

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Memories

Array types • Modelling memories • IP Generators • Instantiating generated components • Implementing ROMs

Basic TEXTIO

TEXTIO • READ and WRITE • Using TEXTIO for testbench stimulus and outputs • STD_LOGIC_TEXTIO

Pre-cursor courses

- Essential Digital Design Techniques (2 days)

Related courses

- Advanced VHDL (Intermediate Level)
- Designing with Quartus II
- SoPC with NIOS II
- Expert VHDL (incorporating Design and Verification modules)

Project services

Doulos Project Services enable clients to access our world-leading technical know-how and apply it directly to projects. **Expert-on-call**, **Expert-design** and **Expert-support** options can be flexibly packaged and delivered to provide valuable expertise and additional resource just when it is needed.

How to book a course

To make a provisional booking, or to obtain pricing information, please contact your local Doulos sales team. You will find contact details on our [website](#).

For further information contact your local Doulos [Sales Office](#).

