

VHDL for FPGA QuickStart

Level: Familiarisation

Duration: 1 day

Heard about VHDL and want to know more? Want to use VHDL but don't know where to start? Do you want to use FPGAs, but feel intimidated? If you answered "yes" to any of these questions then **VHDL for FPGA Quickstart** is for you!

This one day hands-on tutorial will show you how to get started with VHDL and Xilinx FPGAs and whet your appetite for more. You will:

- Understand the basic structure of Xilinx FPGAs
- Learn how VHDL is used to capture and simulate your FPGA design
- See how the Xilinx ISE software implements your design, step by step
- Program the FPGA on a development board

Who should attend?

- Managers who want to understand more about the process of creating FPGA designs and VHDL
- Analogue or Systems designers who work with digital design teams
- Digital designers thinking about making the first moves to VHDL and FPGA design

Prerequisites

No prior experience of VHDL or Xilinx FPGAs and software is needed. You should have a basic understanding of digital logic design, and be computer-literate.

Structure and content

Getting Started with VHDL

What is an FPGA? • What is VHDL? • Tools for FPGA design • How does VHDL affect my design style? • Design flow • Design entity • Ports • Signals • STD_LOGIC • Signal assignment • Processes • Hierarchy • Testbenches • Simulation with ModelSim

LAB: Simulating a binary counter, using ModelSim

Using the Xilinx ISE Software

Xilinx ISE software • Creating a project • Constraints for timing and pins • Implementing a design using the ISE software • Gate-level simulation

LAB: Implementing counter using ISE, and programming a development board

Writing VHDL for Synthesis

Summary of VHDL constructs and their synthesis • Creating finite state machines Synchronous and Asynchronous controls • The NUMERIC_STD package

LAB: Modifying the counter, re-implement and re-program the FPGA

Where do I go from here?

Summary and conclusions • Doulos VHDL, and FPGA training roadmap

